# High Electron Mobility SiGe/Si Transistor Structures on Sapphire Substrates

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## ABSTRACT

SiGe/Si n-type modulation doped field effect structures and transistors (n-MODFETs) have been fabricated on r-plane sapphire substrates. The structures were deposited using molecular beam epitaxy, and antimony dopants were incorporated via a delta doping process. Secondary ion mass spectroscopy (SIMS) indicates that the peak antimony concentration was approximately $4x10^{19}$ $cm^{-3}$. The electron mobility was over 1,200 and 13,000 $cm^2$/V-sec at room temperature and 0.25 K, respectively. At these two temperatures, the electron carrier densities were 1.6 and $1.33x10^{12}$ $cm^{-2}$, thus demonstrating that carrier confinement was excellent. Shubnikov-de Haas oscillations were observed at 0.25 K, thus confirming the two-dimensional nature of the carriers. Transistors, with gate lengths varying from 1 micron to 5 microns, were fabricated using these structures and dc characterization was performed at room temperature. The saturated drain current region extended over a wide source-to-drain voltage ($V_{DS}$) range, with $V_{DS}$ knee voltages of approximately 0.5 V and increased leakage starting at voltages slightly higher than 4 V.

## INTRODUCTION

SiGe/Si n-MODFET structures on sapphire substrates are being studied for potential use in applications that require integration of high frequency RF and digital circuitry on a single wafer. For example, significant cost and performance advantages in Ka-band (26.5 – 40 GHz) transceivers for broadband beam steerable phased array antennas are anticipated by increasing the level of integration. This goal places stringent demands on the substrate material. For the analog circuitry, the substrate must support transistor structures with sufficiently high carrier mobilities to operate at these frequencies, as well as be sufficiently resistive so as to provide electrical isolation between devices [1]. Since most of the device functions are performed in the digital realm, the substrate must also support low-power digital device circuitry [2]. We believe that sapphire is promising for high frequency, high bandwidth system-on-a-chip applications. Complementary metal oxide semiconductor (CMOS) digital circuitry using Si-on-sapphire technology has been widely used for digital signal processing applications where radiation hardness and low power consumption are critical [3,4]. For high frequency system-on-a-chip designs, the performance of passive components such as inductors often limits system performance, and the ability of fabricate high quality inductors on sapphire has been demonstrated [5,6]. A key factor which has limited the upper frequencies at which conventional silicon-on-sapphire (SOS) circuitry can be used is the low carrier mobility. For SOS, the carrier mobility decreases as the silicon thickness and carrier concentration increase, thus all three parameters must be known so as to arrive at meaningful comparisons between transistor technologies. The maximum carrier mobility in a 500 nm thick SOS film was 400 $cm^2$/V-sec, at a sheet carrier density of $2.6x10^{12}$ $cm^{-2}$ [7]. This mobility range is too low for Ka-band circuitry.

The goal of this work is to develop high mobility SiGe/Si structures that will enable SOC integration of Ka-band circuitry onto sapphire substrates.

## EXPERIMENTAL

SiGe/Si n-MODFET growth on r-plane sapphire substrates was accomplished using a multi-step process. First, commercial r-plane sapphire substrates with 270 nm thick Si films were obtained from St. Gobain Crystals, Inc. The crystalline quality of the Si films was improved using a solid phase epitaxy and regrowth process. In our study, Si ions were implanted into the Si films at a dose of $2x10^{15}$ $cm^{-2}$ and a beam energy of 180 keV. The samples were annealed for three hours at 1100 °C in flowing $N_2$, followed by an eight hour $O_2$ anneal, also at 1100 °C. The oxide was chemically etched to achieve a 100 nm thick Si layer. The SiGe buffer layer, virtual substrate, and n-MODFET structures were deposited using molecular beam epitaxy (MBE). A schematic drawing of the various layers is shown in figure 1. The 600 nm thick $Si_{0.7}Ge_{0.3}$ virtual substrate was grown at 755 °C. The 10 nm thick Si channel and 5 nm thick top SiGe spacer layers were grown at 500 °C. Antimony (Sb) was incorporated into the donor layer via a delta-doping approach using an $Sb_4$ source, immediately following growth of the top $Si_{0.7}Ge_{0.3}$ spacer layer. The delta-doped Sb layer deposition was also performed at 500 °C. Next, the substrate temperature was decreased to 200 °C for seven seconds and a thin (~ 1 nm) $Si_{0.7}Ge_{0.3}$ layer deposited, so as to minimize Sb segregation. The substrate temperature was increased to 500 °C and the remaining 9 nm of the donor layer and 5 nm Si cap layer deposited. The microstructural properties of the transistor structures were analyzed using secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM), high resolution x-ray diffractometry (HRXRD), and atomic force microscopy (AFM). Hall effect measurements to measure electron mobility and carrier concentration were made at room temperature and 250 mK. Shubnikov-de Haas data were also taken at 0.25 K. Transistors with gate lengths ranging from 1 microns to 5 microns were fabricated and the DC properties measured. The source and drain regions were prepared by implanting phosphorous ions at a dose of $2x10^{15}$ $cm^{-2}$ and beam energy of 25 keV. The gates were formed by depositing a 300 Å thick layer of platinum, followed by a 3000 Å gold layer.

## RESULTS AND DISCUSSION

Development of high mobility SiGe/Si n-MODFET transistors on r-plane sapphire substrates was accomplished in three stages: materials characterization, Hall mobility measurements, and transistor fabrication. Data highlighting the results obtained in each area is shown below.

### Materials growth and characterization

To achieve high mobility n-MODFET transistor structures on r-plane sapphire, the key microstructural features included optimization of crystalline quality in the virtual substrate and n-MODFET layers, minimization of threading dislocations into the Si channel, sharp, well-defined and smooth SiGe/Si interfaces, a tensile strained Si channel, and donor atoms in the SiGe layer adjacent to the strained Si. The improvement in crystalline quality of the Si and SiGe films was measured using HRXRD ω-rocking curve scans of the symmetric (004) and asymmetric (2 -2 4)

peaks. The full-width half-maximum (FWHM) value of the (004) Si peak for the as-received 270 nm thick Si layer was 0.42°. After the Si implant, $N_2/O_2$ anneal, and chemical etching, the FWHM of the remaining 100 nm thick film decreased to 0.20°. After growth of the SiGe graded buffer layer and virtual substrate, the FWHM of the $Si_{0.7}Ge_{0.3}$ layer dropped to 0.17°. HRXRD rocking curve data after growth of the n-MODFET structure is shown in Figure 2. Cross-sectional transmission electron microscopy of the SiGe graded buffer layer and virtual substrate are shown in Figure 3a. This figure shows dislocation propagation is effectively blocked at the virtual substrate/graded buffer layer interface, and the density of threading dislocations that propagate to the Si channel is approximately $1x10^8$ $cm^{-2}$. High resolution TEM imaging of the n-MODFET portion of the device is shown in Figure 3b, and illustrates sharp, well-defined SiGe/Si interfaces and smooth layer formation. AFM measurements after chemical etching of the SOS layer (prior to MBE growth of the graded SiGe, virtual $Si_{0.7}Ge_{0.3}$ substrate and SiGe/Si n-MODFET) indicated the rms surface roughness was 3.3 nm. After MBE growth, the surface roughness was 3.1 nm, indicating negligible change. SIMS data from the n-MODFET portion of the device is shown in Figure 4. Well-defined $Si_{0.7}Ge_{0.3}$ layers on both sides of the Si channel are clearly observable. Also evident is the Sb peak, demonstrating that the delta doping approach was successfully used to incorporate donor ions near the SiGe/Si interface, and the peak Sb concentration was
$4x10^{19}$ $cm^{-3}$.

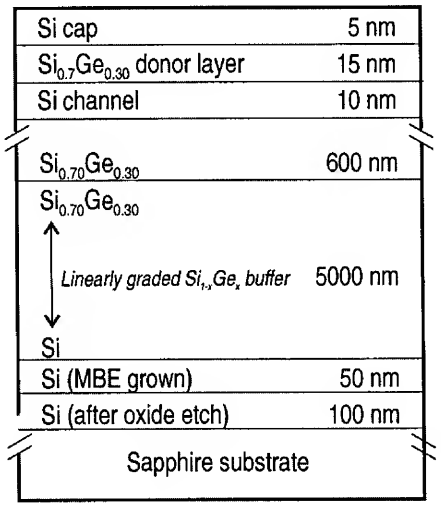


Fig. 1. Schematic diagram of buffer layer, virtual substrate, and n-modulation doped field effect transistor (n-MODFET) structure on r-plane sapphire substrate.

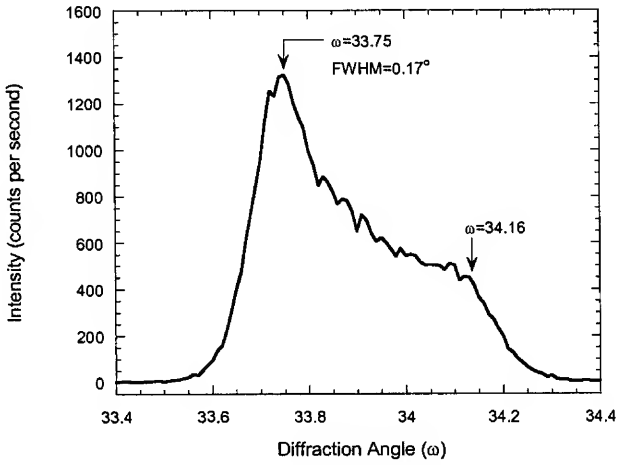


Fig. 2. $\omega - 2\theta$ scan of $Si_{0.7}Ge_{0.3}$ (004) peak. The broad portion extending to $\omega$=34.16° is due to varying Ge concentration in the graded SiGe buffer layer.

**Hall mobility measurements**

Hall effect measurements to measure electron mobility and carrier concentration were made at room temperature and 0.25 K. Shubnikov de-Haas data were also taken at 0.25 K, and data is shown in figure 5. The high room temperature mobility (1,271 $cm^2$/V-sec), coupled with the

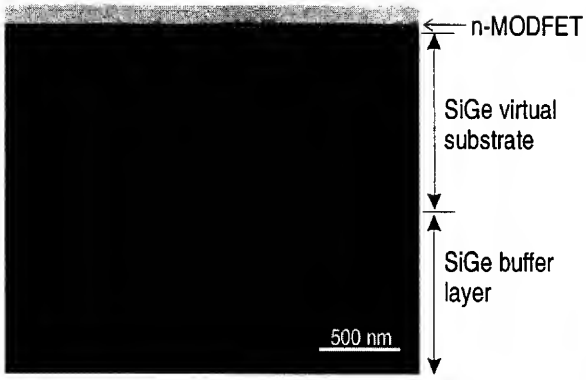


Figure 3a. Cross-sectional TEM of top portion of graded SiGe buffer layer and $Si_{0.7}Ge_{0.3}$ virtual substrate, magnified at 23 kX.

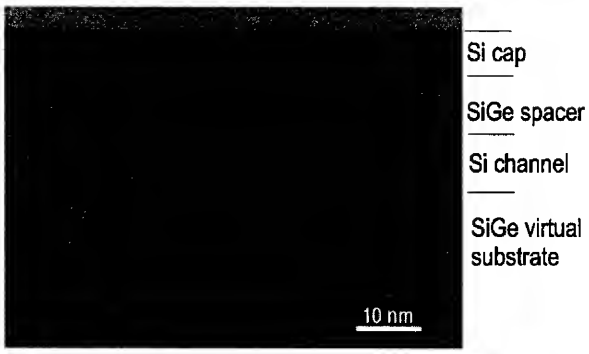


Figure 3b. Cross-sectional TEM of the n-MODFET portion of the device, magnified at 590 kX.

reasonably high carrier density of $1.6x10^{12}$ $cm^{-2}$ and short surface-to-channel distance (20 nm) makes these structures attractive for high frequency system-on-a-chip applications. At 0.25 K, the mobility was 13,313 $cm^2$/V-sec. Although Si films deposited directly on sapphire are compressively stressed [8], the high mobility demonstrated by the n-MODFET devices of this study indicate that the buffer layer and virtual substrate were capable of supporting growth of the high quality, tensile-strained Si channels necessary for 2DEG formation and high electron mobility. For comparison, the bulk mobilities of Si and $Si_{0.7}Ge_{0.3}$, doped to $1x10^{18}$ $cm^{-3}$, are less than 300 $cm^2$/V-sec [9, 10]. At 0.25 K, the electron carrier concentration was $1.33x10^{12}$ $cm^{-2}$. The fact that the carrier concentration at cryogenic temperatures was almost as high as the room temperature indicates excellent carrier confinement. The presence of Shubnikov-de Haas oscillations confirms that the structure operates as a two-dimensional electron gas. In addition, the SdH derived 2DEG carrier concentration is equal, to within experimental error, to the Hall concentration, showing that all the carriers observed at low temperature are in the channel. A more comprehensive report detailing the mobility behavior of these structures is published elsewhere [11]. Other samples from the same wafer gave room temperature mobilities up to 1,380 $cm^2$/V-sec with an accompanying electron carrier concentration of $1.8x10^{12}$ $cm^{-2}$.

**DC transistor performance**

The SiGe/Si n-MODFET structures on r-plane sapphire were used to fabricate prototype transistors. The gate lengths ranged from 1 to 5 $\mu$m. For transistors with 1 or 2 $\mu$m gate lengths, there were 2 $\mu$m gaps between the source and gate, and 2$\mu$m gaps between the gate and drain regions. For transistors with 3 or 5 $\mu$m gate lengths, there were 3 $\mu$m gaps between the source and gate, and 3$\mu$m gaps between the gate and drain regions. The gate widths for all transistors were 100 $\mu$m. The transistors used a double-gate design, wherein gate regions were located on both sides of the drain terminal, and source regions were located adjacent to the gate, on the sides opposite the drain. The transistor's current/voltage characteristics were measured on a Tektronix 370A curve tracer and the connections to the transistors were made through 150 micron pitch Ground/Signal/Ground microwave probes. The DC behavior of a 5 $\mu$m gate length transistor is shown in Figure 6. This data is from the first set of transistors fabricated using these

high mobility SiGe/Si n-MODFET on r-plane sapphire structures. The gate-to-drain and gate-to-source forward bias voltage was measured to be 0.32 V; thus, although the transistors are depletion mode devices, a maximum $V_{GS}$ of +0.3 V was used to increase the $I_{DS}$. The pinchoff current at $V_{GS}$=-0.7 V and $V_{DS}$=2.5 V was 0.0035 mA. The I-V behavior indicated the saturated drain current region extended over a wide source-to-drain voltage ($V_{DS}$) range, with knee voltages of approximately and 0.5 V, flat I-V curves, and increased leakage starting at voltages slightly higher than 4 V. The saturation drain currents were lower than expected, and reasons for this are under investigation.

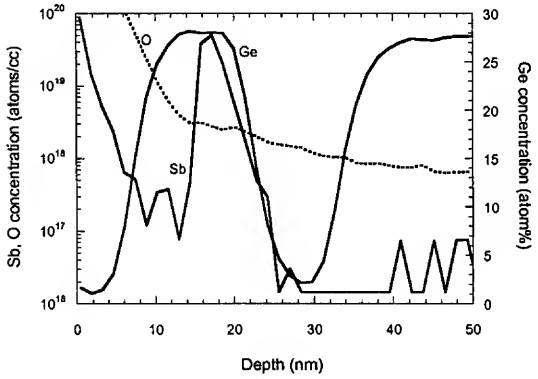


Fig. 4. Secondary ion mass spectroscopy of n-MODFET portion of device.

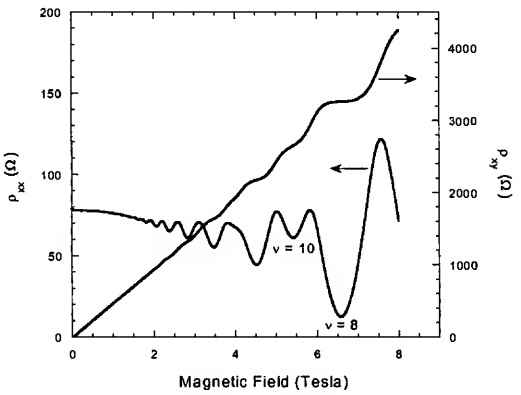


Fig. 5. Longitudinal ($\rho_{xx}$) and Hall ($\rho_{xy}$) resistivity versus magnetic field (T). Data taken at 0.25 K.

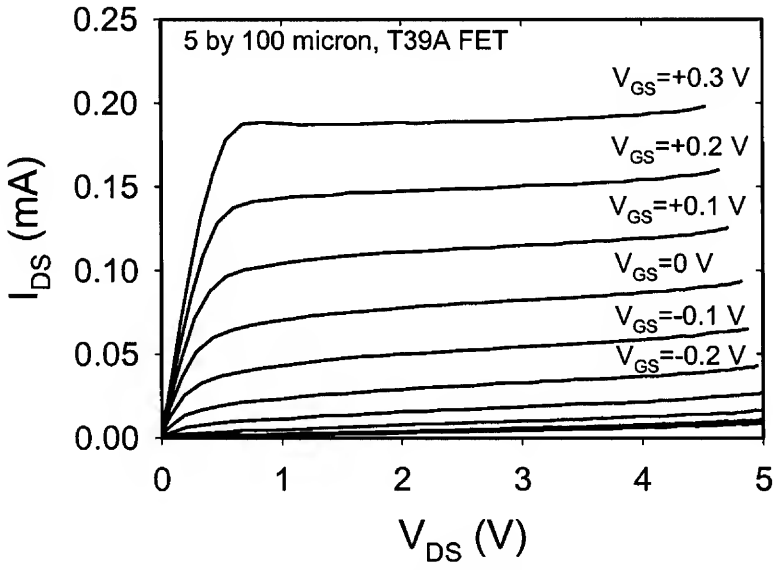


Fig. 6. DC Drain current versus drain voltage for different gate voltages. Gate length = 5 $\mu$m, channel length = 11 $\mu$m, and gate width = 100 $\mu$m.

## CONCLUSIONS

We have demonstrated SiGe/Si n-MODFET structures on r-plane sapphire with electron mobilities over 1200 and 13,000 $cm^2$/V-sec at room temperature and 0.25 K, respectively. Microstructural analysis indicates that MBE growth of SiGe buffer layers and virtual substrates provided a suitable template for growth of a MODFET structure with a 10 nm thick tensile strained channel. A delta doping approach was used to introduce Sb dopants into the structure, and the ability of the MODFET structure to confine carriers within the Si channel was excellent. Transistors fabricated using these structures were normally on, and operated over a gate voltage range of +0.3 to -0.4 volts. The knee voltages for these transistors was ~ 0.5 $V_{DS}$ and leakage was only apparent when $V_{DS}$ was increased above 4 V.

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